REMARKS

Claims 1-4, 8, 16 and 31-33 are pending in the current application. Claim 1 is an independent claim.

35 U.S.C. § 103 (a) Caletka in view of Yoshikawa

Claims 1-4, 16 and 31-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Caletka in view of Yoshikawa. Applicant respectfully traverses this art grounds of rejection.

Caletka discloses a heat-sink or thermally conductive member (e.g., 22, 122, etc.) mounted on top of a semiconductor chip (e.g., 12, 212, 512, etc.). Figure 10 illustrates the steps involved in mounting the heat sink on top of the semiconductor chip. In Step 42 of Figure 10, Caletka discloses positioning the heat sink (alternatively referred to as a thermally conductive member) above the semiconductor chip and held in a mold (e.g., 26, 526, etc.). The preferred method of holding the heat sink in place in the mold and above the semiconductor chip is with a vacuum. Caletka states "the thermally conductive member, held in the mold, preferably by vacuum (vacuum ports 43)" (see column 8, lines 44-45). Caletka further discloses maintaining the heat sink above the semiconductor chip with a thermally conductive material, or alternatively, an adhesive (see column 8, lines 49-53). However, it is clear that the adhesive, which is directed to a non-preferred embodiment disclosed by Caletka, is not applied across the entirety of the semiconductor chip. For example, Caletka states "a small space may be left between the lower surface of the thermal conductive member and the planar upper surface of the chip without thermally conductive material present" (column 8, lines 52-55 of Caletka). While this statement is directed to "thermally conductive material", it follows that this statement also holds true to the embodiment

employing the adhesive because the adhesive is given as an alternative example to the thermally conductive material.

Further, with respect to Step 44 of Figure 10, Caletka discloses inserting a dielectric material into "at least a portion of the upper surface of the circuitized substrate and against the one edge surface of the thermal conductive member and against one edge surface of the chip" (column 8, lines 56-60). Since the dielectric material is inserted/injected and is in direct contact with the chip, the adhesive disclosed by Caletka clearly cannot be positioned across an entirety of the upper surface of the semiconductor chip.

Moreover, the Caletka reference is very ambiguous with regard to the application of the adhesive as employed to hold the heat sink to the semiconductor chip. For example, none of Figures 1-9 illustrate the adhesive. Further, Caletka states the "a significant advantage is obtained by practicing the invention in this manner, eliminating a separate step of attaching a thermal conductive member with a thermal conductive material or adhesive" (see column 9, lines 11-15). Due to Caletka's limited disclosure with regard to the adhesive and its clear inclusion in the Specification as a non-preferred alternative embodiment, Applicant respectfully submits that Caletka cannot disclose or suggest "an adhesion layer disposed between an entirety of the second side of semiconductor chip and at least a portion of the protective cap" as recited in independent claim 1. Further, the combination of Caletka and Yoshikawa likewise cannot disclose or suggest this feature because the Examiner acknowledges that Yoshikawa "fails to teach an adhesion layer disposed between the second side of the semiconductor chip and the protective cap. As a matter of fact, the reference appears to be [silent] as to the material for the space between the second side of the semiconductor chip 3 and the protective cap 1 (see page 6 of the Office Action).

As such, claims 2-4, 16, 31-33 are likewise allowable over Caletka in view of Yoshikawa at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

35 U.S.C. § 103(a) Yoshikawa in view of Caletka

Claims 1-4, 16 and 31-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa in view of Caletka. Applicant respectfully traverses this art grounds of rejection.

As discussed above, the combination of Caletka in view of Yoshikawa cannot disclose or suggest the features present in independent claim 1. Likewise, it follows that the combination of Yoshikawa in view of Caletka also cannot disclose or suggest the features as described above with respect to independent claim 1.

As such, claims 2-4, 16 and 31-33, dependent upon independent claim 1, are allowable over Yoshikawa in view of Caletka at least for the reasons given above with respect to independent claim 1.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

Reconsideration and issuance of the present application is respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-4, 8, 16 and 31-33 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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